HBT BALLAST DESIGN

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BACKGROUND

In order to understand ballast effects in combinations of HBT cells, first consider the Ebers-Moll relationship between Ic and Vbe given in (1). This is also commonly seen in the more compact form of (2), where Is represents the forward saturation current, η is the junction ideality, and V_T is 26mV at room temperature.

Eq.1 $$I_C = Is\left(e^{\frac{Vbe}{\eta V_T}} - 1\right), \quad V_T = \frac{k\,T}{q}$$

Eq.2 $$I_E \approx Is\; e^{\frac{Vbe}{\eta V_T}}$$

Eq.3 $$Vbe = \eta\, V_T \ln\left(\frac{Ie}{Is}\right)$$

Eq.4 $$Vbe = \eta\, V_{To}\, \ln\left(\frac{Ie}{Is_o}\right) - \phi\,\Delta T\ ,$$

where $\phi = -\frac{d\,Vbe}{dT}$, $V_{To} = V_T\,|_{25\mathrm{C}}$, and $Is_o = Is\,|_{25\mathrm{C}}$

Equation 3 is obtained from (2) by taking the log of both sides. The temperature sensitivity of Vbe is pivotal in the proper design of ballast networks for HBT devices. In equation 4, the term $-\phi\,\Delta T$ has been added to equation 3, evaluated at $T = 25C$. Figure 1 shows Vbe for an M14, 270um^2 cell over a range of emitter currents.

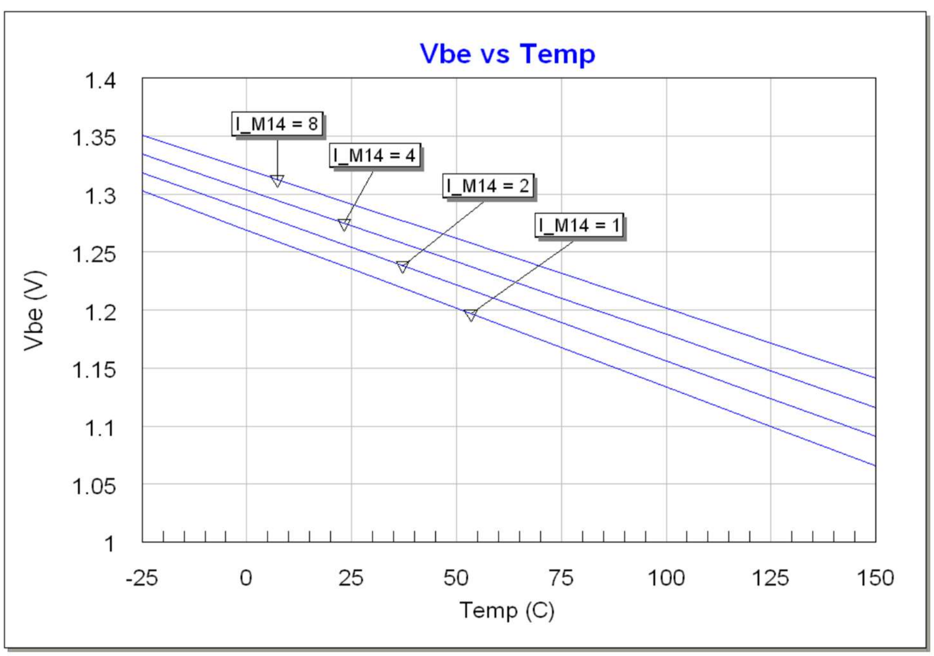

Fig.1 Temperature sensitivity of Vbe for various emitter currents (M14 cell)

The temperature dependence of ϕ is well behaved and essentially constant. Clearly, the current dependence of ϕ is weak, since the slope is nearly constant as the current is varied over three octaves. A practical value for ϕ is 1.3 mV/C from the slope in figure 1. This approach leads to a straight forward way to calculate ballasting levels. The alternative is to deal with the temperature dependence of V_T and Is in equation 3. These are given in equations 5 and 6, and illustrated in figures 2 and 3. While V_T increases linearly, Is exhibits a very nonlinear increase as temperature is increased. The dominant effect is the exponential. When Vbe is expressed functionally, a log function is applied to Is. Fortunately, the inverse functionality of $log_e\left[e^{\left[\frac{T_1}{T_o}\right]}\right]$ allows the well behaved linear ϕ behavior seen in Figure 1.

Eq.5 $$V_T\,(T_1) = V_T\,(T_o)\,\left(\frac{T_1}{T_o}\right)$$

Eq.6 $$Is(T_1) = Is(T_o)\left(\frac{T_1}{T_o}\right)^{X_{TI}} e^{\left[\frac{-Eg(T_O)}{V_T\,(T_O)}\right]\left[1-\frac{T_1}{T_O}\right]}$$, for constants Eg and X_{TI}.

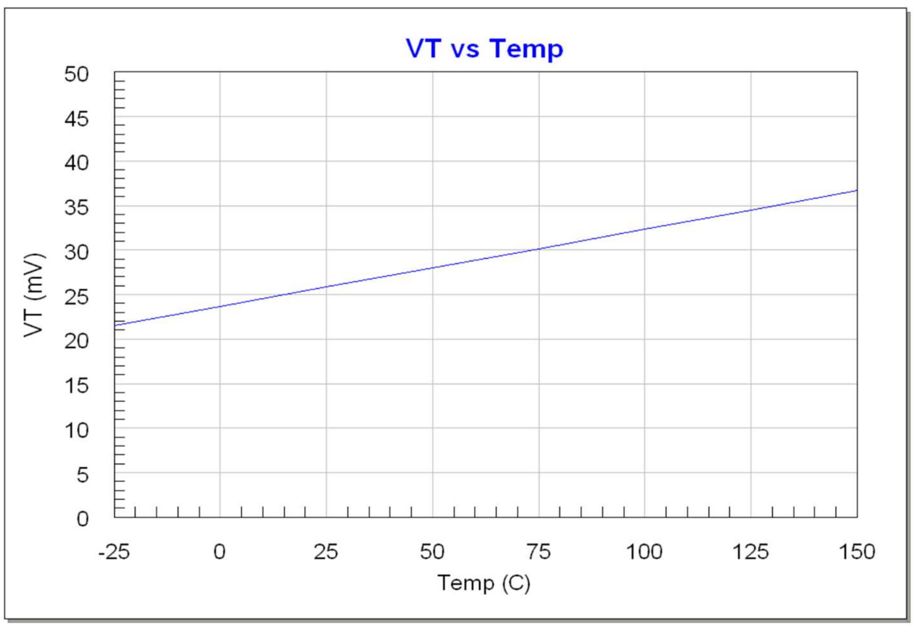

Fig.2 Temperature dependence of V_T

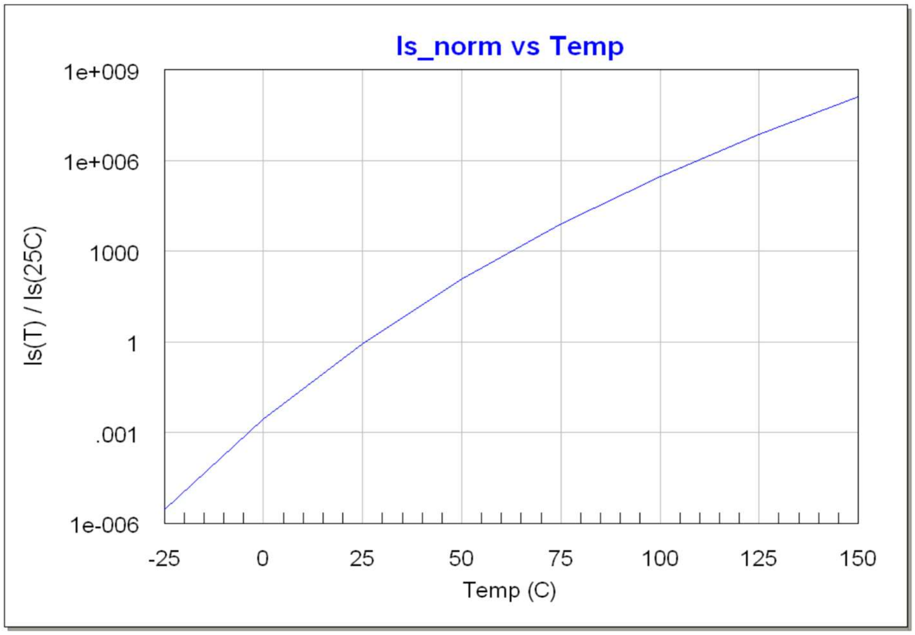

Fig.3 Temperature dependence of Is (normalized to room temp value)

EMITTER BALLASTING

If the reduction in Vbe with increasing temperature is compensated by a degenerative voltage increase, thermal stability can be achieved with an individual transistor. A resistor in the common emitter terminal can provide this.

When two or more transistors are operated in parallel, self heating due to $(Vce\ I_C)$ will cause Vbe to fall by 1.3mV/C from the initial ambient level. If the pair of transistors are operated without mutual thermal coupling, any imbalance in junction temperature can lead to an imbalance in the sharing of collector current, since the pair share the same $\mathrm{V_{BE}}$. This leads to an escalation in the imbalance due to the enhanced imbalance in self heating. The result is a 'hogging' of the collector current by one transistor. If many cells are operated in parallel, the effect can be more dramatic. Not only can the local concentration of heating lead to device failure, collapse of current gain will result. β of HBT devices falls with increased junction temperature. This difference from Silicon BJT devices is both a blessing and a curse. It is responsible for the effective use of base ballasting in GaAs HBT circuits; but, it also leads to current collapse when non-uniform sharing of collector current occurs. Figure 4 illustrates the dependence of β on junction temperature.

Ballasting is essential in circuits with HBT cells connected in parallel. Consider the circuit shown in figure 5. The pair of transistors with emitter resistors can later be generalized to more devices. The common resistor contributes to the overall thermal stability of the aggregate of cells. It does not provide ballasting between cells. Individual emitter resistors are needed at each device to balance current sharing.

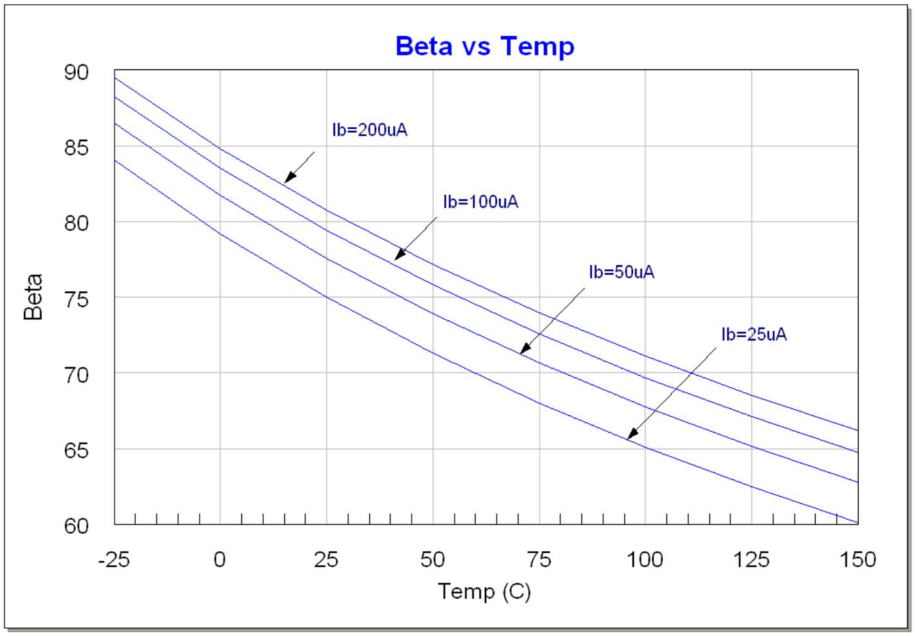

Fig.4 Temperature dependence of β shown for various current levels

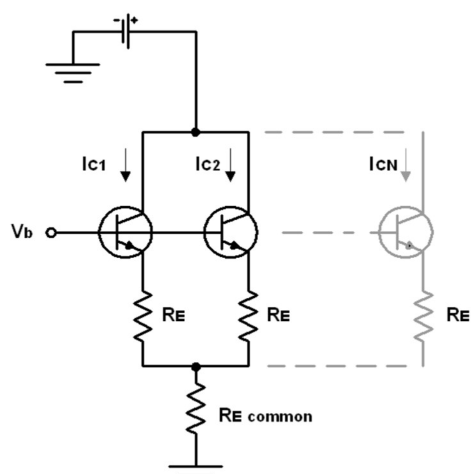

Fig.5 Emitter ballasted HBT pair

Equations 7 and 8 represent equation 4 applied to the left and right cells in figure 5, respectively.

Eq.7 $$Vbe_1 = \eta\, V_{To}\, \ln\left(\frac{I_{E1}}{Is_o}\right) - \phi\, \Delta T_1$$

Eq.8 $$Vbe_2 = \eta\, V_{To}\, \ln\left(\frac{I_{E2}}{Is_o}\right) - \phi\, \Delta T_2$$

By inspection, from figure 5 we obtain equation 9.

Eq.9 $$Vbe_1 - Vbe_2 = I_{E2}R_E - I_{E1}R_E$$

Next, equations 7 and 8 are substituted into (9) to obtain (10).

Eq.10 $$\eta\, V_{To}\left[\ln\left(\frac{I_{E1}}{Is_o}\right) - \ln\left(\frac{I_{E2}}{Is_o}\right)\right] + \phi(\Delta T_2 - \Delta T_1) = I_{E2}R_E - I_{E1}R_E$$

The thermal model for the HBT pair is represented in figure 6. Equations 11 through 13 relate the difference in junction temperatures to the difference in dissipated power between the pair of cells.

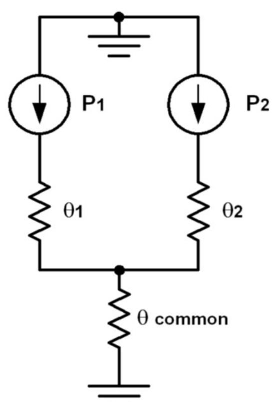

Fig.6 Thermal model for HBT pair

Eq.11 $$\Delta T_1 = (\theta_1 + \theta_{common})P_1 + \theta_{common}\, P_2$$

Eq.12 $$\Delta T_2 = (\theta_2 + \theta_{common})P_2 + \theta_{common}\, P_1$$

Eq.13 $$\Delta T_2 - \Delta T_1 = \theta_2\, P_2 - \theta_1\, P_1$$

The common thermal resistance contributes to the nominal junction temperature and overall thermal instability; but not to any thermal imbalance between the two HBTs. The more tightly coupled (thermally) the cells, the smaller the difference in junction temperatures.

Eq.14 $$\Delta T_2 - \Delta T_1 = \theta_i\,(P_2 - P_1)\ , \quad \text{where} \quad \theta_i = \theta_1 = \theta_2$$

Equation 15 is obtained by substituting (14) into (10).

Eq.15 $$\eta\, V_{To}\left[\ln\left(\frac{I_{E1}}{Is_o}\right) - \ln\left(\frac{I_{E2}}{Is_o}\right)\right] + \phi\,\theta_i(P_2 - P_1) = R_E\,(I_{E2} - I_{E1})$$

Eq.16 $$P_2 - P_1 = V_{CE}\,(I_{E2} - I_{E1}), \qquad V_{CE1} \approx V_{CE2}$$

Eq.17 $$\eta\, V_{To}\left[\ln\left(\frac{I_{E1}}{Is_o}\right) - \ln\left(\frac{I_{E2}}{Is_o}\right)\right] + \phi\,\theta_i V_{CE}\,(I_{E2} - I_{E1}) = R_E\,(I_{E2} - I_{E1})$$

Eq.18 $$\eta\, V_{To}\,\ln\left(\frac{I_{E1}}{I_{E2}}\right) + (\phi\,\theta_i V_{CE} - R_E)(I_{E2} - I_{E1}) = 0$$

Eq.19 $$\eta\, V_{To}\,\ln\left(\frac{I_{E1}}{I_{E2}}\right) + (\phi\,\theta_i V_{CE} - R_E)\left(1 - \frac{I_{E1}}{I_{E2}}\right) I_{E2} = 0$$

Eq.20 $$I_{E2} = \frac{\eta\, V_{To}\,\ln\left(\frac{I_{E1}}{I_{E2}}\right)}{(R_E - \phi\,\theta_i V_{CE})\left(1 - \frac{I_{E1}}{I_{E2}}\right)}$$

Equation 20 represents an HBT pair in the operating region of current collapse. The critical (maximum) value of I_{E2} at the point of collapse is found by considering the limit of (20) as $I_{E1} \to I_{E2}$.

Eq.21 $$I_{E_{MAX}} = \lim_{\gamma \to 1} \frac{\eta\, V_{To}\,\ln(\gamma)}{(R_E - \phi\,\theta_i V_{CE})(1-\gamma)}\ , \quad \text{where } \gamma = \frac{I_{E1}}{I_{E2}}.$$

Eq.22 $$I_{E_{MAX}} = \lim_{\gamma \to 1} \frac{\eta\, V_{To}\,\gamma^{-1}}{(R_E - \phi\,\theta_i V_{CE})(-1)}\ , \quad \text{from L'Hopital's rule}\,.$$

Eq.23 $$I_{E_{MAX}} = \frac{\eta\, V_{To}}{(\phi\,\theta_i V_{CE} - R_E)}$$

Equation 23 represents the critical (maximum) current per cell with an uncoupled thermal resistance, θ_i. Since we are typically interested in the maximum total current for the array of cells, (23) can be rewritten as (24), where I_{MAX} represents the total current and θ represents the aggregate uncoupled thermal resistance (parallel paths) across the array.

Eq.24 $$I_{MAX} = \frac{\eta\, V_{To}}{(\phi\,\theta\, V_{CE} - R_E)}$$

This expression allows emitter ballasting to be designed. As long as $R_E \leq \phi\, \theta\, V_{CE}$, a maximum stable current can be calculated. If $R_E > \phi\, \theta\, V_{CE}$, the ballasting level is considered complete (safe). Both ϕ and θ are weak functions of I_{TOTAL} for a fixed V_{CE}. Figure 1 shows a decrease in ϕ, while the thermal resistivity of GaAs increases with temperature. The two effects are in opposite directions. A conservative approach to the practical use of equation 24 is to use values of ϕ associated with moderate current levels and values of θ from the higher dissipation region.

BASE BALLASTING

As discussed earlier, and illustrated in figure 4, HBT β decreases as junction temperature increases. This behavior makes base ballasting effective in HBT devices. Base current flowing through a dedicated series base resistance, R_B , have the same degenerative effect as an emitter resistance of $R_E = R_B/(\beta + 1)$. Equation 25 is obtained from (24) by adding a base ballast term (in the emitter equivalent form).

Eq.25
$$I_{MAX} = \frac{\eta\, V_{To}}{(\phi\, \theta\, V_{CE} - R_E - R_B/(\beta+1))}$$

If β expansion was present, as in Silicon BJTs, self heating would cause a loss of base ballast effectiveness. This can immediately be seen from the emitter equivalent $R_B/(\beta + 1)$. The fact that β contracts with temperature in HBT devices gives some enhancement to the effectiveness of base ballast.

CELL SIZE

Suppose the array represented by figure 5 represents a single cell. The transistor segments become small subcells instead of individual cells. It is useful to think of HBT cells as comprised of parallel connected, unballasted, small subcells. Without ballasting (within the cell), equation 25 requires the uncoupled thermal resistance to be essentially zero. If local hot spots are allowed, current 'hogging' within the cell can occur. Small cells are the only way to insure uniform temperatures within the cell. The fact that measured SOA correlates inversely with cell size is a direct consequence. Flip chip operation brings better thermal paths; but the trends with cell size remain.

SOME CONSTANTS

If you wish to use (25), you may find the following useful:

$$\eta = 1.1$$

$$V_{To} = 26 \text{ mV}$$

$$\phi = 1.3 \text{ mV/C}$$

REFERENCES

[1] G. Massobrio andP. Antognetti, "Semiconductor Device Modeling with Spice", 2nd ed., McGraw-Hill 1993, Chapter 2.

[2] I. Getreu, "Modeling the Bipolar Transistor", 1st ed., Tektronix 1976, Chapter 2.

[3] W. Liu, "Handbook of III-IV Heterojunction Bipolar Transistors", 1st ed., John Wiley & Sons 1998, Chapter 6.